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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,567	09/12/2003	Kouji Saitou	12480-000021/US	5299

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HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 8910
RESTON, VA 20195

EXAMINER	
HOLTON, STEVEN E	

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/660,567	SAITOU ET AL.	
	Examiner	Art Unit	
	Steven E. Holton	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 6-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 6-13* is/are rejected.

7)☒ Claim(s) *2* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is made in response to applicant's amendment after final filed on 8/1/2007. Claims 1-3 and 6-13 are currently pending in the application. An action follows below:

Response to Amendment

2. The submitted amendments to the claims overcome the rejections made in the previous action. In order to present more a more complete rejection based on the arguments and amendments presented the finality of that action is withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3 and 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi et al. (USPN: 7084849), hereinafter Noguchi, in view of Koyama (USPN: 6600465).

Regarding claim 1, Noguchi discloses an active matrix display device (Fig. 1) with common electrodes (Fig. 17, elements 628 and 629) and source electrodes (Fig. 16, element 608). Noguchi further provides means to match the center of the voltage

waveforms of the common electrode and source electrodes in both reflective and transparent display modes (Fig. 20; col. 35, line 53 – col. 36, line 13). This inherently requires some sort of applying this voltage to the electrodes. Further, Noguchi provides each pixel with a switching element (Fig. 1, element 20). The switching elements produce a variation in voltage on the source electrode line when in an ON or OFF state. This voltage variation is caused by gate-drain capacitance, which is parasitic capacitance, and Noguchi applies a correction voltage to the electrodes to remove visual flicker caused by parasitic capacitance by matching the center voltages of the common and source electrodes (col. 35, lines 13-62).

However, Noguchi does not expressly disclose if the offset voltage is generated or stored by the display before being applied to the signals applied to the electrodes.

Koyama discloses a liquid crystal display device that measures a offset value to be applied to display electrodes of the device. The offset voltages are stored in a memory device (Fig. 1, element 103) and then read from the memory to be applied to the correct electrodes (col. 3, lines 50). Koyama also discusses that the storage device could be either a digital memory or an analog circuit to generate the offset voltage (col. 3, lines 19-28).

At the time of invention it would have been obvious to one skilled in the art to modify the teachings of Noguchi with the teachings of Koyama to produce a device as described in claim 1. A digital memory device as described by Koyama could be used to store offset voltages that would be read out for the purpose of matching the center voltages of the common and source electrodes as used by Noguchi. Noguchi does not

describe how the offset voltages are generated or stored and thus, any reasonable method of providing offset voltages to electrodes could be used by one skilled in the art. One such known and reasonable method of providing offset voltages to electrode waveforms for display devices is a digital memory as shown by Koyama. Thus, it would have been obvious to one skilled in the art to modify the teachings of Noguchi with the teachings of Koyama to produce a device as described in claim 1.

Regarding claims 3 and 9, Noguchi discloses using an offset voltage to match the center of voltage waveforms applied to the signal and common electrodes and the shift does not include a change of the amplitude of the voltage waveform being shifted (col. 38, lines 18-39).

Regarding claims 6-8, the Examiner notes that the claims merely disclose methods of storing voltage signal information in a memory device. Storing a voltage signal based on a minimum, maximum, or average value of the signal along with a value representing the amplitude of the overall signal would have been obvious to one skilled in the art when storing a data signal for later reproduction. It would have been obvious that any data signal with a varying voltage level would require some storage of the maximums, minimums, starting points or ending points of the signal and some method of determining the changes and frequency or other information about the data signal. Therefore, storing a voltage signal holding a minimum voltage and change of signal would be obvious in order to reproduce the signal from memory when applied to an electrode.

Regarding claim 10, the display device of Noguchi includes thin film transistors (Fig. 1, element 20; col. 11, line 55) the transistors are connected to signal lines, gate signal lines and connected to the pixel as is common in active matrix display devices. The matching of the centers of the signal and common electrode waveforms is used to overcome a voltage that is stored in the pixel because of parasitic capacitance between components of the pixel (col. 35, lines 22-40).

Regarding claim 11, the display of Noguchi is a dual-mode display that operates with a reflective and trasmissive mode of operation (col. 2, lines 32-46).

Regarding claim 12, the correction voltages of Noguchi are not indicated as being determined multiple times, but are only read from storage to the appropriate electrodes to correct flicker in the display. Therefore, it is inherent that the correction voltages are only determined once in the manufacture of the display device.

Regarding claim 13, Noguchi shows different voltages and correction voltages being applied to electrodes in the transmissive and reflective modes of operation (Fig. 20).

Allowable Subject Matter

4. Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Claim 2 recites the limitation applying the shifting voltage waveform to the common electrode of the display for each display mode. The closest prior art, Noguchi, discloses applying a correction voltage to a source electrode line while maintaining the voltage of the common electrode line, and does not anticipate or render obvious the underlined features.

Response to Arguments

5. Applicant's arguments, see pages 6-13, filed 8/1/2007, with respect to the rejection(s) of claim(s) 1-3 and 6-13 under 35 USC 112 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Noguchi in view of Koyama under 35 USC 103(a) as discussed above.

Regarding the arguments that Noguchi does not correct for parasitic capacitance of the thin film transistors the Examiner again notes col. 35, lines 13-52. The gate-drain capacitance Cgd creates voltage differences between the ON and OFF states of the TFT. This gate-drain capacitance is parasitic capacitance. Noguchi then provides an offset voltage to prevent flicker caused by the 'feedthrough voltage' by shifting the center voltages of the source electrode waveforms. This is the parasitic voltage compensation presented in the disclosed invention.

The Examiner points out that the disclosed invention appears to utilize a single common electrode and to either shift the center voltage of either the source electrodes or the common electrode waveform to correct for flicker caused by parasitic capacitance

from within the thin film transistors and based on the display mode of the display device. Noguchi discloses a display device containing two common electrodes each common electrode specific to a transmissive area or a reflective area of the display device, and corrects for flicker caused by parasitic capacitance by shifting the center voltage of the source electrode waveforms. The inventions both contain the concept of correcting flicker caused by parasitic capacitance by providing a correction voltage to shift center voltages so that the center voltages of waveforms match.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven E. Holton whose telephone number is (571) 272-7903. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven E. Holton
Division 2629
August 17, 2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER